



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

Address: COMMISSIONER FOR PATENTS

P.O. Box 1450

Alexandria, Virginia 22313-1450

www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/532,904	04/27/2005	Peter-Andre Redert	NL 021087	3107
24737 7590 01/29/2009 PHILIPS INTELLECTUAL PROPERTY & STANDARDS P.O. BOX 3001 BRIARCLIFF MANOR, NY 10510				
EXAMINER				
HAJNIK, DANIEL F				
ART UNIT		PAPER NUMBER		
2628				
MAIL DATE		DELIVERY MODE		
01/29/2009		PAPER		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

### Office Action Summary

**Application No.**

10/532,904

**Applicant(s)**

REDERT ET AL.

**Examiner**

DANIEL F. HAJNIK

**Art Unit**

2628

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 20 November 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-17 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SG/US)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

**Claims 1-15** rejected under 35 U.S.C. 103(a) as being unpatentable over Gelsey (US Pat. No. 6,344,837), in view of Norman (US Pat. No. 6,154,855).

#### ***Regarding Claim 1.***

Gelsey discloses a method for visualization of a 3-dimensional (3-D) image comprising:  
converting a 3-D scene model into a plurality of 3-D scene points;  
(See e.g. col. 9 lines 4-5) into a plurality of 3-D scene points (See e.g. col. 9 lines 4-10  
where the 3-D scene point is the point where R intercepts S. See also e.g. Figs 1, 2 and 3);  
providing at least a portion of the plurality of 3-D scene points to a 3-D display plane  
comprising 3-D pixels that are directionally modulated (See e.g. col. 9 lines 25-29, where SP =  
scene point, and DMP = 3-D pixel);  
calculating a contribution of light from the 3-D pixel to generate at least in part a scene  
point of the plurality of 3-D scene points (in figure 7 where the cube is a directionally modulated  
pixel or 3-D pixel; in this figure, the point source of light is 15; a scene point is shown in figure 8

for objects 4, 6, and 8; a scene point is any individual point representing part of the object surface or definition as shown; in figure 8, a plurality of directionally modulated pixels or 3-D pixels are located in image display device IDD 26);

performing at least one of emitting and transmitting the light by each of the 3-D pixels (See e.g. Fig 3 block 10 and Fig. 4A and See e.g. Abstract, "each directionally-modulated pixel is provided by locating a point source of light behind a microminiature array of liquid crystal device (LCD) elements, each of which are operated by a control device programmed to vary the light transmission characteristics of each element at a given time ").

Gelsey does not explicitly disclose the claimed "calculating at each of the 3-D pixels a contribution of light" because in Gelsey this calculation is performed at a central processor and not at each individual 3-D pixel (col 8, lines 26-36 and in figure 13).

Norman teaches the use of arrays of local processors for display, with explicit calculation of input (See e.g. Norman col. 2 lines 30-45, col. 7 lines 38-46, col. 9 lines 13-21 and col. 9 ll. 4-10 "...each array cell having access to a global input and having direct optical output means as well as minimal memory and processing means, allowing the array to receive, decompress and display data transmitted by another apparatus, such as a computer..."). Here, each cell receives global data and performs calculations to determine its output.

It would have been obvious to those having ordinary skill in the art at the time of invention to modify the determination of the contribution of light at each of the 3-D pixels of Gelsey to calculate locally as in Norman. It was known that incorporating a complete miniature data processing system in this manner can have the advantage of overcoming I/O and memory

bottlenecks by providing a massively parallel data processing system (See e.g. Norman col. 9 ll. 28-37).

Gelsey is modified by Norman by incorporating one cell in the array of local processors of Norman into each 3-D pixel in Gelsey to perform calculation rather than at their central processor. Gelsey can be modified according to the following passages in the reference: (*Gelsey: col 5, lines 39-43, "The modulation of each of the modulation regions 16 is controlled by an appropriate control system such as one or more computer processors in conjunction with suitable interface circuitry" and Gelsey: col 4, lines 31-35, "As shown in the latter, the DMPs 14 are configured in rows and columns with minimum spacing therebetween. Note also that the electronic circuitry for controlling the modulation of the DMPs 14 is also contained within the IDD 12"*). In this case, Gelsey states that more than one processor may be used with the system. Norman provides an array of processors. In addition, Gelsey states that electronic circuitry for each DMP (directionally modulated pixel or 3-D pixel) is already present in the IDD (image display device). Thus, since some of the circuitry is already present this would make it easier to modify Gelsey to incorporate the array of processors as disclosed by Norman because each processor would need to communicate with the pixel by way of circuitry.

***Regarding Claim 2.***

Gelsey discloses the method according to claim 1, wherein light is emitted and/or transmitted by 2-D pixels comprised within said 3-D pixels, each 2-D pixel directing light into a different direction contributing light to a scene point of said 3-D scene model.

(See e.g. Gelsey col. 4 line 54 through col. 5 line 8 especially “centrally located point source of light within ... modulation regions” and “light emitted in different directions having the different visual properties appropriate for the scene being displayed.” The claimed 2-D pixels are also shown in figure 7 as rectangular or square modulation regions 24)

***Regarding Claim 3.***

Gelsey does not explicitly disclose the method according to claim 1, wherein said 3-D scene points are provided sequentially, or in parallel, to said 3-D pixels.

However, Norman teaches the use of parallel arrays of processors (See e.g. Norman col. 2 lines 30-45, col. 7 lines 38-46 and col. 9 lines 13-21).

It would have been obvious to those having ordinary skill in the art at the time of invention to modify the display method of Gelsey to provide 3-D scene points to 3-D pixels sequentially or in parallel as in Norman. It was known that a highly parallel data processing system can have the advantage of overcoming the I/O and memory bottlenecks that plague parallel processors as well as the von Neumann bottleneck of single processor architectures (See e.g. Norman col. 9 lines 27-36).

***Regarding Claim 4.***

Gelsey discloses the method according to claim 1, wherein the calculation of the contribution of light of a 3-D pixel to a certain 3-D scene point is made previous to the provision of said 3-D scene points to said 3-D pixels.

(See e.g. Gelsey col. 10 lines 1-11, "However, all computations to display a given set of 3D scenes can be done in advance and stored for later playback". See also Fig. 14, where scene point SP is set equal to Intercept (R,S) in block 72, followed by provision of the scene points to the 3-D pixel in block 74 by setting the modulation region to match SP).

***Regarding Claim 5.***

Gelsey does not explicitly disclose all the claimed limitations.

The combination of Gelsey and Norman teaches the claimed: method according to claim 1, wherein the contribution of light of a 3-D pixel to a certain 3-D scene point is calculated within one 3-D pixel of one row or of one column previous to the provision of said 3-D scene points from the one 3-D pixel to the remaining 3-D pixels of a row or a column, respectively.

The combination of Gelsey and Norman also teaches the claimed:

(Norman teaches of intercell communication in a single row, i.e. see figure 1B where cell S communicate data to adjacent cell A in the same row; Gelsey teaches of calculating a contribution of light of a 3-D pixel as follows: in the abstract, "Each directionally-modulated pixel (DMP) emits light which is modulated in a manner that is not uniform in all directions, to insure that the light emitted in each included direction is appropriate for the scene being displayed"; when these two references are combined as the claimed features are taught).

It would have been obvious to one of ordinary skill in the art to use the intercell communication in a row as taught by Norman with the 3D pixel array in Gelsey in order to reduce errors and reduce bandwidth in any one individual cell by considering neighboring cells (abstract of Gelsey).

**Regarding Claims 6 and 7.**

Gelsey does not explicitly disclose all the claimed limitations.

The combination of Gelsey and Norman teaches the claimed: the method according to claim 1, wherein a 3-D pixel outputs an input 3-D scene point to at least one neighboring 3-D pixel (*where Gelsey shows a 3-D pixel, a cubic directionally modulated pixel, in figure 7; Norman shows how the output of one cell may become the input of an adjacent or neighboring cell in figure 1D. This connection between cells, i.e. cell S and cell A, which share a common row, establishes intercell communication. When the two references are combined, all the claimed features are taught*) and teach the claimed: the method according to claim 1, wherein each 3-D pixel alters the co-ordinates of a 3-D scene point prior to putting out said altered 3-D scene point from each 3-D pixel to at least one neighboring 3-D pixel (*where Gelsey shows a 3-D pixel, a cubic directionally modulated pixel, in figure 7 and 3-D scene points in figure 8 where the shapes projected from screen 26 are made of a plurality of scene points; in figure 8, each 3D pixel affects the coordinates or position of the 3-D scene shapes because the 3-D pixels are located inside screen 26; Norman shows how the output of one cell or pixel may alter data of an adjacent or neighboring cell in figure 1D. This connection between cells, i.e. cell S and cell A, which share a common row, establishes intercell communication. When the two references are combined, all the claimed features are taught*).

In regards to claims 6 and 7, it would have been obvious to one of ordinary skill in the art to use the intercell communication in a row as taught by Norman with the 3D pixel array in



Gelsey in order to reduce errors and reduce bandwidth in any one individual cell by considering neighboring cells (abstract of Gelsey).

***Regarding Claim 8.***

Gelsey discloses the method according to claim 1, wherein if more than one 3-D scene point needs the contribution of light from one 3-D pixel, the depth information of said 3-D scene point is decisive (*See e.g. col. 4 lines 49-53 where occlusion depends on viewing direction.*)

***Regarding Claim 9.***

Gelsey discloses the method according to claim 1, wherein 2-D pixels of the 3-D display plane transmit and/or emit light only within one plane. (*See e.g. col. 6 lines 1-24, esp. 18-19, also see figure 7, where the rectangular or square modulation regions 24 emit light only within one plane as shown because the front surface of the cubic directionally modulated pixel is flat.*)

***Regarding Claim 10.***

Gelsey discloses the method according to claim I, wherein color is incorporated by spatial or temporal multiplexing within each 3-D pixel (*See e.g. col. 5 lines 8-24 and Fig. 5. See also col. 5 lines 55-65 where the RGB, red blue green, color components are multiplexed.*)

***Regarding Claim 11.***

The reasons and rationale for the rejection of claim 1 is incorporated herein.

Gelsey does not explicitly disclose: wherein said 3-D pixels comprise an input port and an output port for receiving and putting out 3-D scene points of a 3-D scene. However, the combination of Norman and Gelsey teaches such an arrangement (Norman: col. 32 lines 13-20, also see figure 1D where the cells in grid each represent a pixel, and each cell has their own input and output ports, i.e. cell S has output to cell A and cell A can input from cell S; Gelsey also provides part of the claimed feature by teaching of 3-D pixels that each make up a cell, i.e. see figure 7 where the cube represents one 3D pixel).

It would have been obvious to persons having ordinary skill in the art at the time of invention to modify the 3-D pixel of Gelsey to incorporate an input and an output port as in Norman. It was known that having cells equipped with direct input and direct output means allows the array to handle input intensive tasks without encountering an input bottleneck (See e.g. Norman col. 32 lines 22-25.)

#### ***Regarding Claim 12***

As per claim 12, this claim is similar in scope to claims 3 and 7, and thus is rejected under the same rationale.

#### ***Regarding Claim 13.***

Gelsey teaches the 3-D display device according to claim 11, wherein said 3-D pixels comprise a spatial light modulator with a matrix of 2-D pixels. (See e.g. Gelsey Fig. 5, in particular, the numerous modulation regions 16; in this case the modulation regions 16 are the

claimed matrix of 2-D pixels and the claimed 3-D pixel is the directionally modulated pixel 14).

***Regarding Claim 14.***

Gelsey teaches the 3-D display device according to claim 13, wherein said 3-D pixels comprise a point light source, providing said 2-D pixel with light (See e.g. Gelsey 3-D display 26 in figure 8; also see figure 7 which shows a 3-D pixel 14 with a point source of light 15, the 2D pixels are shown as rectangular or square modulation regions 24).

***Regarding Claim 15.***

Gelsey does not explicitly disclose the 3-D display device according to claim 13, wherein said 3-D pixels comprise registers for storing a value determining which ones of said 2-D pixels within said 3-D pixel contribute light to a 3-D scene point.

However, Norman teaches the use of arrays of processors where each processor has its own memory (See e.g. Norman Fig. 10 block 1016 where this memory is a plurality of registers, see also col. 2 lines 30-34.)

It would have been obvious to persons having ordinary skill in the art at the time of invention to modify the value determination of pixel contribution of light to a 3-D scene point as in Gelsey to incorporate storage registers as taught by Norman. It was known that systems comprising arrays of processors where each processor has its own memory can have the advantage of removing the von Neumann uni-processor bottleneck and the multi-processor memory bottleneck for parallel applications (See e.g. Norman col. 2 lines 34-36).

**Claims 16 and 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Gelsey (US Pat. No. 6,344,837) in view of Norman (US Pat. No. 6,154,855) and Seitz, et al. (US Pat. No. 6,363,170).

***Regarding Claim 16.***

Gelsey does not explicitly disclose the method of claim 1, wherein the calculating of the contribution comprises calculating whether a current 3-D scene point is closer to a viewer than a past 3-D scene point.

However, See e.g. Seitz, et al. col. 6 line 66 - col. 7, line 7. Here, voxel processing involves 1-bit Z-buffering, or occlusion detection which determines whether the current scene pixel is closer to a viewer than the previous 3-D scene point.

It would have been obvious for persons having ordinary skill in the art to modify the contribution calculation of Gelsey to determine relative depth of a scene point as taught by Seitz et al. It was known that use of depth testing can have the advantages of reducing required processing and preventing display of hidden surfaces.

***Regarding Claim 17.***

Gelsey does not explicitly disclose the 3-D display device of claim 11, wherein the control unit calculates whether a current 3-D scene point is closer to a viewer than a past 3-D scene point.

However, See e.g. Seitz, et al. col. 6 line 66 - col. 7, line 7. Here, voxel processing involves 1-bit Z-buffering, or occlusion detection which determines whether the current scene pixel is closer to a viewer than the previous 3-D scene point.

It would have been obvious for persons having ordinary skill in the art to modify the contribution calculation of Gelsey to determine relative depth of a scene point as taught by Seitz et al. It was known that use of depth testing can have the advantages of reducing required processing and preventing display of hidden surfaces.

#### ***Response to Arguments***

1. Applicant's arguments filed 11/20/2008 have been fully considered but they are not persuasive.

Applicant argues that the combination of references

It is respectfully submitted that it is improper to use the teaching of the present application as a source of teachings for rendering the present application unpatentable. The section of the present application cited in the Office Action, namely page 2, lines 18-21, is a section that describes the present invention and accordingly, use of this section in rejecting the present claims is improper use of hindsight reconstruction ...

Norman is cited for "[teaching] the use of arrays of local processors for display, with explicit calculation of input" (see, Office Action, bottom of page 3 continuing to page 4, line 2 ) , however, it is respectfully submitted that reliance on Norman is misplaced. What in fact Norman

shows is merely a fault tolerant parallel processor system enabled "to receive, decompress and display a large number of parallel input streams . . ." (See, Norman, Col. 9, lines 19-20.) (pages 9-11 in filed response).

The examiner respectfully maintains that the rejections are proper because the passage in question was cited merely as an aid for explanation. The quotation as argued has been removed in this office action in order to avoid any future confusion.

Furthermore, the prior art combination is based upon obviousness-type rationale and not impermissible hindsight of applicant's disclosure. For example, in the office actions, Norman is relied for teaching the concept of parallel processing. Applicant's invention appears to be an obvious variation of the display system as described in Gelsey. For example, many similar techniques are used in Gelsey (such as modulation of light rays) in order to achieve an autostereoscopic display (3D volumetric display). Norman is cited to show that increased perform using hardware at the pixel or cell level with multiple processors is known in the art. In order words, one can take a system and add more processing power to it in order to improve performance. Such techniques are known in the art and constitute a "common sense" approach to improving performance.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the

applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Applicant remarks:

Gelsey performs the 3-D calculation at a central processor and transfers the data to the 3-D pixels for rendering a scene. Norman merely shows a parallel processing system and each of the 3-D pixels calculating a contribution of light from the 3-D pixel, and as such, does nothing to cure the deficiencies in Gelsey.

(pages 12-13 in filed response).

In this instance, the examiner respectfully believes the rejection statement is proper because Gelsey does teach the claimed concepts of: calculating a contribution of light from the 3-D pixel to generate at least in part a scene point of the plurality of 3-D scene points. For example, see the following in the reference: *(in figure 7 where the cube is a directionally modulated pixel or 3-D pixel; in this figure, the point source of light is 15; a scene point is shown in figure 8 for objects 4, 6, and 8; a scene point is any individual point representing part of the object surface or definition; in figure 8, a plurality of directionally modulated pixels or 3-D pixels are located in image display device IDD 26)*. Gelsey does not explicitly disclose the claimed "calculating at each of the 3-D pixels a contribution of light" because in Gelsey this calculation is performed at a central processor and not at each individual 3-D pixel (col 8, lines 26-36 and in figure 13). However, when taken in combination using cell network of Norman, all the claimed limitations are met.

Gelsey is modified by Norman by incorporating one cell in the array of local processors of Normal to each 3-D pixel in Gelsey to perform calculation rather than at their central processor. Gelsey can be modified and suggests the combination according to the following passages in the reference: (*Gelsey: col 5, lines 39-43, "The modulation of each of the modulation regions 16 is controlled by an appropriate control system such as one or more computer processors in conjunction with suitable interface circuitry" and Gelsey: col 4, lines 31-35, "As shown in the latter, the DMPs 14 are configured in rows and columns with minimum spacing therebetween. Note also that the electronic circuitry for controlling the modulation of the DMPs 14 is also contained within the IDD 12"*). In this case, Gelsey states that more than one processor may be used with the system, not just a central processor. Norman provides an array of processors. In addition, Gelsey states electronic circuitry for each DMP (directionally modulated pixel or 3-D pixel) is already present in the IDD (image display device). Thus, an existing circuitry infrastructure is already present at the 3-D pixel level, this would make obvious to modify Gelsey to incorporate the array of processors as disclosed by Norman. Thus, the combination is obvious to one of ordinary skill in the art.

Applicant remarks:

Although Gelsey is cited for showing these features, it is respectfully submitted that since it is undisputed that Gelsey fails to disclose or suggest calculating at each of the 3-D pixels a contribution of light from the 3-D pixel . . . , it is unsupportable that Gelsey discloses or suggests the features of claims 5, 6 and 7  
(middle of page 13 in filed response).



In this instance, the examiner respectfully believes the rejection statement is proper because the combination of both Gelsey and Norman are relied upon for teaching these claimed features. For example, Gelsey shows a 3-D pixel, a cubic directionally modulated pixel, in figure 7; Norman shows how the output of one cell may become the input of an adjacent or neighboring cell in figure 1D. This connection between cells, i.e. cell S and cell A, which share a common row, establishes intercell communication. When these two references are combined, all the claimed features are taught.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel F. Hajnik whose telephone number is (571) 272-7642. The examiner can normally be reached on Mon-Fri (8:30A-5:00P).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Xiao Wu can be reached on (571) 272-7761. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Daniel Hajnik/  
Patent Examiner  
Art Unit 2628